UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,417	12/17/2004	Syuichi Kikuchi	30391-18	6771

7590 02/21/2007

Mitchell P Brook
Luce Forward Hamilton & Scripps
11988 El Camino Real
Suite 200
San Diego, CA 92130

EXAMINER	
PARIKH, KALPIT	
ART UNIT	PAPER NUMBER
2187	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,417	KIKUCHI, SYUICHI	
	Examiner	Art Unit	
	Kalpit Parikh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :17 December 2004, AND 6 July 2006 .

DETAILED ACTION

The instant application having Application No. 10/518417 has a total of 31 claims pending in the application; there are 3 independent claims and 28 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. ' 1.63**.

II. STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required by **M.P.E.P. ' 201.14(c)**, acknowledgment is made of applicant's claim for priority based on both 371 of PCT/JP03/07672 filed on June 17 2003 AND Japanese Patent Application No. 2002-178674 filed on June 19 2002.

III. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

As required by **M.P.E.P. ' 609 (C)**, the applicant's submission of the Information Disclosure Statements dated July 6 2006, and December 17 2004 are acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P. ' 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

IV. REJECTIONS NOT BASED ON PRIOR ART

IVa. DEFICIENCIES IN THE CLAIMED SUBJECT MATTER

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 29-31 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claim recites a computer program for allowing a computer to realize a disclosed functionality.

Claims 29-31 are drawn to a computer program per se (i.e., computer program not claimed as embodied in computer-readable storage media). It appears that the computer program recited in claims 29-31 only recite a set of instructions capable of being executed by a computer, the computer program itself is not a process and, as such, represents nonstatutory functional descriptive material per se because computer programs per se are not capable of causing functional change in the computer. See, e.g., Warmerdam, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure per se held nonstatutory). Such claimed data structures do not define any structural and functional interrelationships between the data structure and other claimed aspects of the invention which permit the data structure's functionality to be realized. In contrast, a claimed computer-readable medium encoded with a data structure defines structural and functional interrelationships between the data structure

and the computer software and hardware components which permit the data structure's functionality to be realized, and is thus statutory.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1-31 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. There appear to be numerous instances within the claims where the recited claim elements either appear to lack antecedent basis, or it is unclear which element is being referenced. What follows are some examples of instances that are representative of such deficiencies.

Claims 5 and 7-25 recite the limitation "those targets" in claims 5,7 and 8. There is insufficient antecedent basis for this limitation in the claims.

Claim 8 recites, "that page where said to be written data has been written" in line 27 of page 43, however it is unclear, which page the claim is referring to. Claim 1 recites "the empty page" where said to be written data is written to (page 42 line 19), and claim 6 recites, "a page indicated by said physical address" (page 43 line 15).

Claims 8-25 rejected for being indefinite because of the following: The claims appear to recite "that" and "said" interchangeably while to referring to the same claimed element. It is unclear if "that" element and "said" element are referring to the same claimed element. For example, claim 8 (page 43 line 27) recite "a logical

address" and "that page." Claim 8 (page 44 line 2) recites, "said logical address" and "said page." Claim 8 (page 44 line 3) recites "that logical address" and "that page."

Claims 1-25 rejected for being indefinite because of the following: The claims appear to refer to the same claim elements using different terminology. For example, in independent claim 1, a page where to be written data is written to is referred to as "an empty page" (page 42 line 12). In dependent claim 8, a page where to be written data is written to is referred to as "that page." It is unclear if "that page" is referring to the empty page.

Claims 24-25 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The scope of claims 24-25 appears to be unclear because it is unclear which elements the claim is referring to when the claim recites said element (ex/ that page).

V. REJECTIONS BASED ON PRIOR ART

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. **Claims 1-31** provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claims 1-17** of copending **Application No. 11/547181** in view of **Sinclair et al. (US Pat No. 6725321 [PCT Pub Date: 24 August 2000])**.

10/518417	11/547181	Sinclair et a.
Claim 1: a memory device characterized by comprising: a non-volatile memory including	Claim 1: A storage device comprising:	
a plurality of memory blocks for storing data to which physical addresses are allocated each of said blocks including physical pages each of said physical pages including a logical page and a redundancy portion	a storing section (11) including multiple memory blocks as storage areas for storing user data, each memory block being formed by combining multiple groups each having a storage capacity smaller than the memory block, and each group being formed by combining multiple pages each having a storage capacity smaller than the group;	It is well known in the art to include a redundancy portion to a page of a flash memory block in a system as claimed in 11/547181 (see e.g., Sinclair et al. FIG 3: 1b).
a translation table memory (123) which, stores an address translation table (BPT) showing a correlation between physical addresses of pages constituting each of said memory blocks and logical addresses of said pages;	a table storing section (123) that stores a first table (61) for associating a physical group address indicating a physical position of the group in the storage area with a logical group address indicating a logical position of the group;	
a pointer memory (123) which specifies an empty page in a data storable state from among said pages and stores a write pointer (BSI) indicating a physical address of said specified empty page; and	a pointer storing section (123) that obtains an empty group where user data is storable from the group to store a pointer indicating a physical group address of the obtained empty group; and	
a controller (12, S311, S314) which, when this memory system is activated, performs initializing process in which reads data from the redundancy portions of said non-volatile memory and prepares the address translation table in said translation table memory the write pointer in said pointer memory when to-be-written data and a logical address are supplied to said memory device , writes said to-be-written data in the empty page indicated by said write pointer, and renews said address translation table in such a way as to show a correlation between the physical address of that empty page and said logical address	a writing section (12), upon supply of the user data, a logical group address indicating a group in which the user data is to be written, an inner group address indicating a storage position where the user data in a page belonging to the group, that writes the user address at the storage position indicated by the inner group address of the page belonging to the empty group indicated by the pointer and further writes data for associating the physical group address of the empty group with the supplied logical group address in the first table (61).	It is well known in the art to initialize a translation table by reading the redundancy portions of the pages in a flash memory block in a system such as the one claimed in 11/547181 (see e.g., Sinclair et al. COL 5 LINE 64- COL 6 LINES 5).

Claim 1 of Application No. 10/518417 and claim 1 of Application No. 11/518417 are drawn to a memory comprising of blocks with physical addresses, each block comprising of pages, wherein a write pointer and a translation table are used to manage memory access to the memory.

Claim 1 of Application No. 11/547181 does not expressly appear to disclose each page comprises of a logical portion and a redundancy portion as recited in claim 1 of Application No. 10/518417. Nor does claims 1 of Application No. 11/547181 expressly disclose reconstructing the translation table from said redundancy portions of pages as recited in claim 1of Application No. 10/518417.

In the same field of endeavor Sinclair et al. disclose a memory system comprising of the aforementioned elements of claims 1 of Application No. 11/547181 wherein a page of a memory further comprises a logical portion and a redundancy portion. Sinclair et al. further disclose utilizing the redundancy portion of the pages to reconstruct the contents of a write pointer memory and a translation table memory.

Sinclair et al. and Application No. 11/547181 are analogous art because they are from the same field of endeavor namely, nonvolatile memory management.

It would have been obvious to a person of ordinary skill in the art to add a redundancy portion to the pages of a memory system as recited in claims 1 of Application No. 11/547181 to arrive at the invention as recited in claims 1 of Application No. 10/518417.

The suggestion/motivation for doing so would have been for improved system performance as disclosed by Sinclair et al. (see e.g., COL 5 LINE 64- COL 6 LINES 5 AND Abstract).

Therefore it would have been obvious to combine Sinclair et al. with the claims of Application 11/547181 to arrive at the invention as specified in claim 1 of Application No. 10/518417.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claim 1,26 and 29** rejected under 35 U.S.C. 102(b) as being anticipated by **Sinclair et al. (US Pat No. 6725321 [PCT Pub Date: 24 August 2000])**.

As per **claim 1,26 and 29**, Sinclair et al. disclose a memory device characterized by comprising: a non-volatile memory (see e.g., FIG 2: 6) including

- a plurality of memory blocks for storing data to which physical addresses are allocated (see e.g., COL 1 LINES 30-35), each of said blocks including physical pages (see e.g., COL 1 LINES 37-39 "sectors" AND COL 6 LINES 32-34), each of said physical pages including a logical page(see e.g., FIG 6: 1a) and a redundancy portion (see e.g., FIG 6: 1b);
- a translation table memory (see e.g., COL 1 LINES 61-64: "sector allocation table) (123) which, stores an address translation table (BPT) showing a correlation between physical addresses of pages constituting each of said memory blocks and logical addresses of said pages;
- a pointer memory (see e.g., COL 1 LINES 44-46) (123) which specifies an empty page in a data storable state from among said pages and stores a write pointer (BSI) indicating a physical address of said specified empty page; and

- a controller (12, S311, S314) which, when this memory system is activated,
    - o performs initializing process (see e.g., COL 5 LINE 64 - COL 6 LINE 5) in which
    - o reads data from the redundancy portions of said non-volatile memory (i.e., header field) (see e.g., COL 28: LINES 10-13) and
    - o prepares the address translation table in said translation table memory (see e.g., COL 5 LINES 57-60 AND COL 6 LINES 1-5) the write pointer in said pointer memory (see e.g., COL 6 LINES 5-8),
    - o when to-be-written data and a logical address are supplied to said memory device (see e.g., COL 1 LINES 53-55), writes said to-be-written data in the empty page indicated by said write pointer (see e.g., COL 1 LINES 55-59), and
    - o renews said address translation table in such a way as to show a correlation between the physical address of that empty page and said logical address (see e.g., COL 1 LINES 60-67).

[The same reasoning applies mutatis mutandis to the subject matter of independent claims 26 and 29.]

3. **Claim 1-5 AND 26-31** rejected under 35 U.S.C. 102(b) as being anticipated by **Mason (US Pat No. 5740396)**.

As per **claim 1,26 and 29**, Mason discloses a memory device characterized by comprising:

- a non-volatile memory (see e.g., FIG 5: 8A) (11) including a plurality of memory blocks for storing data to which physical addresses area allocated (see e.g., FIG 10: 9A),
    - each of said blocks including physical pages (see e.g., FIG 17: 11 AND 12),
    - each of said physical pages including a logical page(see e.g., FIG 17: 11) and a redundancy portion (see e.g., FIG 17: 12).
    - a translation memory (123) which stores an address translation table (BPT) showing a correlation between physical addresses of pages constituting each of said memory blocks and logical addresses of said pages(see e.g., FIG 15);
    - a pointer memory (123), which specifies an empty page in a data storable state from among said pages and stores a write pointer (BSI) indicating a physical address of said specified empty page (see e.g., COL 6 LINE 67- COL 7 LINE 2); and
    - a controller (see e.g., FIG 5: 4) (12, S311, S314) which, when this memory system is activated,
        - performs initializing process in which reads data from the redundancy portions of said non-volatile memory (see e.g, COL 3 LINES 9-11) and

- prepares the address translation table in said translation table memory and the write pointer in said pointer memory (see e.g., COL 3 LINES 8-11),
- when to-be-written data and a logical address are supplied to said memory device, writes said to-be-written data in the empty page indicated by said write pointer (see e.g., COL 7 LINES 16-21), and
- renews said address translation table in such a way as to show a correlation between the physical address of that empty page and said logical address (see e.g., COL 7 LINES 23-27).

[The same reasoning applies mutatis mutandis to the subject matter of independent claims 26 and 29.]

As per **claim 2,28 and 30**, Mason disclose the memory device according to claim 1, characterized in that said controller (12)

- designates memory blocks from which data is to be erased from among those memory blocks which have data stored therein (S501) and discriminates whether data stored in said designated memory block is valid or not, for each of those pages which constitutes said designated memory blocks, transfers that data which has been discriminated as valid to another memory block, and erases that data which is stored in said designated memory blocks (S503) (see e.g., COL 7 LINES 35-49).

[The same reasoning applies mutatis mutandis to the subject matter of independent claims 28 and 30.]

As per **claim 3,29 and 30** Mason disclose the memory device according to claim 2, characterized in that said controller (12)

- discriminates whether or not the number of those memory blocks which do not have data stored therein becomes a number which does not satisfy a predetermined condition (S317), and
- designates memory blocks from which data is to be erased among data storing memory blocks
- when having discriminated that the number of said memory blocks which do not have data stored therein has become the number which does not satisfy said predetermined condition (S501) (see e.g., COL 7 LINES 35-49).

[The same reasoning applies mutatis mutandis to the subject matter of independent claims 29 and 31.]

As per **claim 4**, Mason disclose the memory device according to claim 3, characterized in that said controller (12)

- writes invalid flag indicating that data stored in a page to which a logical address has been allocated at a time-to-be-written data, and said logical address are supplied to said memory device is invalid in the page once (S310) (see e.g., COL 9 LINES 28-33), and
- said controller (12) designates an oldest-data storing memory block among those data storing blocks which include pages where said invalid flag is

written once, as a memory block form which data is to be erased (S501) (see e.g., COL 7 LINES 35-49 AND COL 9 LINES 20-27).

As per **claim 5**, Mason disclose the memory device according to claim 4, characterized in that said controller (S502, S506)

- eliminates data stored in that page where said invalid flag is written once from those targets which are to be transferred to said another memory block (see e.g., COL 9 LINES 24-27 AND FIG 13: 37).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claim 6-15** rejected under 35 U.S.C. 103(a) as being unpatentable over **Mason (US Pat No. 5740396)** as applied to claim 3 above, and further in view of **Sinclair (US Pat No. 6069827)**.

As per **claim 6**, Mason disclose the memory device according to claim 6, characterized in that

- a physical address includes a block addresses indicating that block to which a page indicated by said physical address belongs (see e.g., FIG 7: PBN-'0'-'4'), and block address are cyclic ordered, and

  [The physical addresses are cyclically ordered because the physical addresses are represented in a binary numbering scheme, wherein incrementing the highest address outputs the first address because the number of bits representing the address are fixed (ex/F+1=0) (see e.g., COL 6 LINES 30-33.]

However, Mason does not expressly disclose

- said controller (S501) designates as a memory block from which data is to be erased, that one of data-storing memory blocks which is or follows a last block where data has been erased and to which a top block address is given.

In the same field of endeavor, Sinclair discloses a system and method for designating

- memory block from which data is to be erased, that one of data-storing memory blocks which is or follows a last block where data has been erased and to which a top block address is given (see e.g., FIG 3a and FIG 3b).

Sinclair and Mason are analogous art because they are from the same field of endeavor namely, memory management in flash memory.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system of Mason by implement a cyclical scheme for deciding which block was to be written/erased next for the benefit of implementing an automatic wear-leveling system as taught by Sinclair (see e.g., COL 3 LINES 19-21).

The suggestion/motivation for doing so would have been to reduce system overhead and improve performance by implementing an automatic wear leveling system that "may achieve 100% efficiency in the use of available FLASH memory capacity"(see e.g., Sinclair COL 3 LINES 24-26).

Therefore it would have been obvious to combine Sinclair with Mason for the benefit of implementing an automatic wear leveling to obtain the invention as specified in the claim.

As per **claim 7**, Mason in view of Sinclair disclose the memory device according to claim 6, characterized in that said controller (12)

- writes an invalid flag indicating that data stored in a page to which a logical address has been allocated at a time to-be-written data and said logical address are supplied to said memory device is invalid in that page once (S310) (see e.g., Mason: COL 9 LINES 28-33), and
- eliminates data stored in that page where said invalid flag is written once from those targets which are to be transferred to said another memory block (S502, S506) (see e.g., Mason: COL 9 LINES 24-27 AND FIG 13: 37).

As per **claim 8**, Mason in view of Sinclair disclose the memory device according to claim 6, characterized in that said controller (12)

- writes a logical address supplied to said memory device in that page where said to-be-written data has been written (S314) (see e.g., Mason: FIG 8: LSA 1->PBN 3 AND BLOCK 3 G->1), and
- discriminates whether or not said logical address stored in said page coincides with that logical address which is associated with the physical address of that page in said address translation table (see e.g., Mason: FIG 13: 39), and
- eliminates data stored in that page from those targets which are to be transferred to said another memory block when having discriminated that there is no coincidence (S501, S502, S506) (see e.g., Mason: FIG 13: 36-38).

As per **claim 9**, Mason in view of Sinclair disclose the memory device according to claim 8, characterized in that

- physical addresses are cyclically ordered, and said pointer memory (123) specifies a top one of those empty pages which are given physical addresses equal to or following the physical address of that page where data is written (see e.g., COL 6 LINE 62-COL 7 LINE 6).

  [The physical addresses are cyclically ordered because the physical addresses are represented in a binary numbering scheme, wherein incrementing the highest address outputs the first address because the number of bits representing the address are fixed (ex/F+1=0) (see e.g., COL 6 LINES 30-33.]

As per **claim 10**, Mason in view of Sinclair disclose the memory device according to claim 9, characterized in that

- when the logical address of a to-be-read page is supplied to said memory device (see e.g., Mason: COL 8 LINES 36-43),
  - a physical address associated with said logical address is specified based on said address translation table (see e.g., Mason: COL 8 LINES 44-45) and
  - data is read out from that page which is indicated by said specified physical address and is sent outside (S206 to S214) (see e.g., Mason: COL 8 LINES 64-65)

As per **claim 11**, Mason in view of Sinclair disclose the memory device according to claim 9, characterized in that

- when the logical address of a to-be-read page is supplied to said memory device, that page which is given said logical address is specified based on said address translation table and data is read out from said specified page and is sent outside (S206 to S214)(see e.g., Mason: FIG 11: 23,24 AND 27).

As per **claim 12,** Mason in view of Sinclair disclose the memory device according to claim 12, characterized in that

- said address translation table shows a correlation between predetermined upper digits of the physical address of each page and the logical address of that page,

  [Pages addresses are sequentially ordered, so the upper digits of the physical address of each page belonging to the same memory block will have the same upper digits (see e.g., FIG 6: 5A 'PBN').]
- said controller (12) writes a logical address supplied to said memory device in that page where said to-be-written data has been written (see e.g., FIG 6: Block 3: 7-G-1); and
- when the logical address of a to-be-read page is supplied to said memory device, a value of said predetermined upper digits of the physical address associated with said logical address is specified based on said address translation table (see e.g., FIG 6: 5A: Block address is specified) and
- data is read out from that page which is included in individual pages each having a physical address whose upper digits coincide with said specified value and in which said logical address of said to-be-read page is written, and

is sent outside (S206 to S214) (see e.g., Mason COL 8 LINE 64 - COL 4 LINE 4).

[Data is read from each page of a block, which contains pages that have a physical address whose upper digits coincide with said specified value.]

As per **claim 13**, Mason in view of Sinclair disclose the memory device according to claim 12, characterized in that said controller (12)

- writes an invalid flag indicating that data stored in a page to which a logical address has been allocated at a time to-be-written data and said logical address are supplied to said memory device is invalid in that page once (S310)(see e.g., Mason: FIG 6: Block 1-1-A AND Block 1-2-A'), and
- data is read out from that page which is included in individual pages each having a physical address whose upper digits coincide with said specified value and in which said logical address of said to-be-read page is written and said invalid flag is not written, and is sent outside (S206 to S214) (see e.g., Mason: COL 7 LINES 55- COL 8 LINE 5 AND COL 6 LINES 48-50).

As per **claim 14,** Mason in view of Sinclair disclose the memory device according to claim 8, characterized in that

- physical addresses are cyclically ordered, said pointer memory (123) specifies a top one of those empty pages which are given physical addresses equal to or following the physical address of that page where data is written (see e.g., COL 6 LINE 66-COL 7 LINE 5), and

- said controller (12) reads out data from a lowest-ordered page in those individual pages each having a physical address whose upper digits coincide with said specified value and in which said logical address of said to-be-read page is written, and sends said data outside (S206 to S214) (see e.g., Mason COL 7 LINE 55- COL 8 LINE 5).

As per **claim 15**, Mason in view of Sinclair disclose the memory device according to claim 11, characterized in that

- said address translation table shows a correlation between predetermined lower digits of the physical address of each page and the logical address of that page, and a range over which a value of a physical address can be associated with a logical address is determined for each logical address, (see e.g., FIG 5A) and

  [The translation table shows a correlation between the lower digits of the physical address and the logical address because the table shows a correlation between the physical address and the logical address.]
- when the logical address of a to-be-read page is supplied to said memory device, said controller (S206 to S214) specifies a value of said predetermined lower digits of the physical address associated with said logical address is specified based on said address translation table (see e.g., FIG 6: 5A LSA->PBN), and
- reads out data from that page which is included in individual pages each having a physical address whose lower digits coincide with said specified

value and which is given a physical address lying in said range (see e.g., Mason FIG 6: 8A Block 3-Pages 7-9), and sends that data outside (see e.g., Mason FIG 6: 8A).

5. **Claim 16-25** rejected under 35 U.S.C. 103(a) as being unpatentable over **Mason (US Pat No. 5740396)** in view of **Sinclair (US Pat No. 6069827)** as applied to claim 15 above, and further in view of **Kikuchi (US Pat No. 6725321 [PCT Pub Date JUN 17 1999)**.

As per **claim 16**, Mason in view of Sinclair disclose the memory device according to claim 15,

However, Mason in view of Sinclair do not expressly disclose

- said translation table memory (123) is constituted by a non-volatile memory which stores said address translation table.

In the same field of endeavor Kikuchi et al. disclose

- said translation table memory (123) is constituted by a non-volatile memory which stores said address translation table (see e.g., Kikuchi COL 2 LINES 19-21.

Kikuchi and Mason in view of Sinclair are analogous art because they are from the same field of endeavor, namely non-volatile memory management.

At the time of invention it would have been obvious to a person of ordinary skill in the art to implement the translation table memory in non-volatile memory instead of volatile memory.

The suggestion/motivation for doing so would have been to eliminate the need for a volatile memory for storing the translation table (see e.g., COL 1 LINES 44-56 AND COL 2 LINES 19-26).

Therefore, it would have been obvious to implement a translation table memory in non-volatile storage in the system of Mason in view of Sinclair for the benefit of eliminating the need for SRAM memory.

As per **claim 17**, Mason in view of Sinclair disclose the memory device according to claim 15,

However, Mason in view of Sinclair do not expressly disclose

- said translation table memory (123) is constituted by the page that stores said address translation table, and
- said controller (S310 to S312) reads at least a part of said address translation table from said page
- renews said read part in such a way as to show a correlation between the physical address of said empty page indicated by said write pointer and said logical address and writes said renewed part in another empty page (S601 to S603).

In the same field of endeavor Kikuchi discloses

- said translation table memory (123) is constituted by the page that stores said address translation table (see e.g., Kikuchi COL 2 LINES 19-41), and
- said controller (S310 to S312) reads at least a part of said address translation table from said page (see e.g., Kikuchi COL 2 LINES 39-41)

- renews said read part in such a way as to show a correlation between the physical address of said empty page indicated by said write pointer and said logical address and writes said renewed part in another empty page (S601 to S603)(see e.g., Kikuchi FIG 10).

  Kikuchi and Mason in view of Sinclair are analogous art because they are from the same field of endeavor, namely non-volatile memory management.

  At the time of invention it would have been obvious to a person of ordinary skill in the art to implement the translation table memory in non-volatile memory instead of volatile memory.

  The suggestion/motivation for doing so would have been to eliminate the need for a volatile memory for storing the translation table (see e.g., COL 1 LINES 44-56 AND COL 2 LINES 19-26).

  Therefore, it would have been obvious to implement a translation table memory in non-volatile storage in the system of Mason in view of Sinclair for the benefit of eliminating the need for SRAM memory.

As per **claim 18**, Mason in view of Sinclair further in view of Kikuchi disclose the memory device according to claim 17, characterized in that said controller (12)

- stores an address translation table storage location list showing physical addresses of those pages which store data constituting said address translation table (S105B) (see e.g., Kikuchi COL 8 LINES 53-64),

- reads at least a part of said address translation table from that page which is given a physical address indicated by said address translation table storage location list (see e.g., Kikuchi FIG 6:103),
- renews said read part in such a way as to show a correlation between the physical address of said empty page indicated by said write pointer and said logical address (see e.g., Kikuchi FIG 12) and
- writes said renewed part in another empty page (see e.g., FIG 10), and
- renews said address translation table storage location list in such a way as to show the physical address of said another empty page (S602, S603) (see e.g., Kikuchi FIG 10 S316).

As per **claim 19**, Mason in view of Sinclair further in view of Kikuchi disclose the memory device according to claim 17, characterized in that

- a range of a value of upper digits of the physical address of each of those pages which store data constituting said address translation table is predetermined (see e.g., Mason FIG 6),
- said controller (12) stores an address translation table storage location list showing predetermined lower digits of the physical address of each of those pages which store data constituting said address translation table (S105B) (see e.g., Mason FIG 6),
- reads at least a part of said address translation table from that page which is included in pages each having a physical address whose predetermined lower digits are specified by said address translation table storage location list

and the predetermined upper digits of the physical address of which lies in said range (see e.g., Mason COL 8 LINE 64 - COL 4 LINE 4).

[Data is read from each page of a block, which contains pages that have a physical address whose upper digits coincide with said specified value.]

- renews said read part in such a way as to show a correlation between the physical address of said empty page indicated by said write pointer and said logical address (see e.g., Mason FIG 5->FIG 6) and
- writes said renewed part in another empty page, and renews said address translation table storage location list in such a way as to show the physical address of said another empty page (S602, S603). (see e.g., FIG 10 S316)

[The flash memory is specified as NAND type, where data writes are executed in empty pages]

As per **claim 20,** Mason in view of Sinclair further in view of Sinclair et al. disclose the memory device according to claim 19, characterized in that said controller (S601 to S603)

- specifies that page which stores a part showing a correlation between said logical address supplied to said memory device and said physical address from among those pages which have said address translation table stored therein (see e.g., Kikuchi COL 8 LINES 53-55),
- reads only that part which is stored in said specified page (see e.g., Kikuchi see e.g., FIG 6),

- renews said read part in such a way as to show a correlation between the physical address of said empty page indicated by said write pointer and said logical address (see e.g., FIG 7 AND FIG 8) and
- writes said renewed part in another empty page (see e.g., FIG 10 S316) [The flash memory is specified as NAND type, where data writes are executed in empty pages]

As per **claim 21**, Mason in view of Sinclair in view of Kikuchi disclose the memory device according to claim 20, characterized by further comprising

- a non-volatile memory (123) which stores an empty block table containing information for identifying that memory block which does not have data stored therein (see e.g., Abstract), and
- in that said controller (12), further, discriminates whether or not writing to-be-written data supplied to said memory device in an empty page has resulted in that the memory block which includes said empty page has no further empty page (see e.g., Mason COL 9 28-37 AND Kikuchi FIG 13), and
- renews said empty block table in such a way as to indicate that said memory block including said empty block has said data stored therein, when having discriminated that said memory block including said empty block has no further empty page (S315, S316) (see e.g., FIG 10 AND FIG 13), and
- renews said empty block table in such a way as to indicate that a memory block from which data to be stored has been erased does not have that data stored therein (see e.g., FIG 10 AND FIG 13).

As per **claim 22**, Mason in view of Sinclair in view of Kikuchi disclose the memory device according to claim 20, characterized in that

- some of said pages constitute empty block table memory means (11) which stores an empty block table containing information for identifying that memory block which does not have data stored therein, and said controller (12) (see e.g., Kikuchi COL 8 LINES 53-64 AND COL 2),
- further, discriminates whether or not writing to-be-written data supplied to said memory device in an empty page has resulted in that the memory block which includes said empty page has no further empty page (see e.g., Mason COL 9 28-37 AND Kikuchi FIG 13), and,
- when having discriminated that there is no further empty page, reads at least a part of said empty block table from said empty block table means, renews said empty block table in such a way as to indicate that said memory block including said empty block has said data stored therein (see e.g., FIG 13),
- and stores said renewed empty block table in said empty block table means (S315, S316) (see e.g., COL 8 LINES 53-64), and
- reads at least a part of said empty block table from said empty block table means, renews said empty block table in such a way as to indicate that a memory block from which data to be stored has been erased does not have said data stored therein, and stores said renewed empty block table in said empty block table means (S504) (see e.g., FIG 10 AND FIG 13).

As per **claim 23**, Mason in view of Sinclair in view of Kikuchi disclose the memory device according to claim 22, characterized in that said controller (12)

- stores an empty block table pointer indicating the physical address of a page storing that data which constitutes said empty block table (S107), and reads at least a part of said empty block table from that page which is given said physical address indicated by said empty block table pointer (see e.g., COL 8 LINES 53-56).

As per **claim 24**, Mason in view of Sinclair in view of Kikuchi disclose the memory device according to claim 22, characterized in that

- a range of a value of upper digits of the physical address of each of those pages which store data constituting said address translation table is predetermined (see e.g., Kikuchi COL 8 LINES 53-56), and
- said controller (12) stores an empty block table pointer indicating predetermined lower digits of the physical address of a page storing that data which constitutes said empty block table (S 107) (see e.g., Kikuchi COL 8 LINES 53-56), and
- reads at least a part of said empty block table from that page which is included in pages each having a physical address whose lower digits are specified by said empty block table pointer and which has a physical address whose upper digits lie in said range (S308). ',

As per **claim 25**, Mason in view of Sinclair in view of Kikuchi disclose the memory device according to claim 24, characterized in that said

- controller (12) specifies that page in which a to-be-renewed part in said stored empty block table is stored from among those pages which have said empty block table stored therein, and reads out only that part which is stored in said specified page (see e.g., Kikuchi FIG 10 AND FIG 13).

VI. **RELEVANT ART CITED BY THE EXAMINER**

The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

The following references teach a **flash memory management system with a write pointer pointing to a page address of a flash memory:**

U.S.PATENT NUMBER	FIGURES
5459850	3C
6430650	1

VII. **CLOSING COMMENTS**

Conclusion

VIIa. **STATUS OF CLAIMS IN THE APPLICATION**

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

VIIb. **CLAIMS REJECTED IN THE APPLICATION**

Per the instant office action, claims 1-31 have received a first action on the merits and are subject of a first action non-final.

VIII. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kalpit Parikh whose telephone number is (571) 270-1173. The examiner can normally be reached on MON THROUGH FRI 7:30 TO 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kalpit Parikh/

Kalpit Parikh
Examiner
Art Unit 2187

6 February 2007

DONALD SPARKS
SUPERVISORY PATENT EXAMINER